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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/522,470	03/09/2000	Hiroshi Katakura	000267	3147

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ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/522,470	KATAKURA ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/8/04; 8/18/04; 8/31/04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7,8,13 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 7 is/are allowed.

6)☒ Claim(s) *1,2,8,13 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/8/04,8/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 08/31/2004.

2. Claims 1-2, 7-8, 13, and 15 are pending in this application. Claims 1-2, 7, 13, and 15 are independent claims. In Amendment, claims 1-2 and 13 are amended; claims 3-6, 9-12, and 14 are cancelled; and claim 15 is added. This action is made final.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 15, the limitation "the first logic level" in line 3 lacks an antecedence basis. For examination purposes, the examiner considers the first logic level as a inverted signal.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2, 8, 13, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Freeman (Re. 34,363).

Re claim 1, Freeman discloses in Figure 2 a logic circuit comprising: a first inversion section (21) for inverting a first input signal (A) a first logic level and outputting an inverted first input signal (bar(A)); a second inversion section (22) for inverting a second input signal (B) having a logic level opposite the first logic level and outputting the inverted signal (bar(B)); and a transmission section (transmission lines that connect all signals to 23-26) for selecting between outputting one of the inverted first input signal of first inversion section (output controls by C2 and bar(C2)) and the inverted second input signal of second inversion section (output controls by C3 and bar(C3)) in response to an externally controllable selection signal (Cs) and an inverted signal of the selection signal (bar(Cs)).

Re claim 2, Freeman discloses in Figure 2 a logic circuit (a portion of Figure 2) comprising a first inversion section (21) for inverting a first input signal (A) and outputting the inverted signal (/A); a second inversion section (22) for inverting a second input signal (B) and outputting the inverted signal (/B); a first outputting section (output of 25) for selecting between outputting one of the output of first inversion section (/A) and the output of second inversion section (/B) in response to an externally controllable first selection signal (C1) and an inverted signal of the first selection signal (/A); and a second outputting section (output of 24) for selecting between outputting one of the output of first inversion section and the output of second inversion section in response to

an externally controllable second selection signal and an inverted signal of the second selection signal (/B and C3).

Re claim 8, Freeman further discloses in Figure 2 comprising a first switching section (area including transmission lines of A, bar(A) and C2, bar(C2)) provided on an input side of first inversion section (21) and capable of performing switching of whether the first input signal should be passed (on) or blocked (off) in accordance with an external control signal (bar(C2)); and a second switching section (area including transmission lines of B, bar(B) and C3, bar(C3)) provided on an input side of second inversion section (22) and capable of performing switching of whether the second input signal should be passed (on) or blocked (off) in accordance with the external control signal (bar(C3)).

Re claim 13, Freeman further discloses in Figure 2 a first inversion section (21) for inverting a first input signal (21) having one of positive logic and negative logic and outputting an inverted first input signal (bar(A)), first inversion section (21) including transistor circuits (col. 4 lines 45-55) each of transistor circuits having a first input signal terminal (input of 21) for the first input signal (A), a first input selection signal terminal (e.g 29c) for the controllable selection signal (e.g C1) and an outputting terminal (input to 23) for outputting the selection signal (C2) or the inverted signal (bar(C2)) based on the logic of the first input signal (A); a second inversion section (22) for inverting a second input signal (B), second inversion section (22) including transistor circuits each (col. 4 lines 45-55) of transistor circuits having a second input signal terminal (input to 22) for the second input signal (B), a second input selection signal terminal (e.g. 29d) for the

controllable selection signal (e.g. C0) and an outputting terminal (input to 25) for outputting the selection signal (C3) or the inverted signal (bar(C3)) based on the logic of the first input signal; and a transmission section (all the connection bus between inverters to other logic components) for selecting between outputting one of the output of first inversion section (21) and the output of second inversion section (22) in accordance with a logical value which depends upon an externally controllable selection signal (C2 and C3) and an inverted signal of the selection signal (bar(C2) and bar(C3)).

Re claim 15, it has similar limitations cited in claim 1. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Allowable Subject Matter

7. Claim 7 is allowed.

Response to Arguments

8. Applicant's arguments filed 08/31/2004 have been fully considered but they are not persuasive.

a. The applicant argued in pages 9 and 11 for independent claims 1-2 that the cited reference by Freeman does not disclose or suggest a transmission section that selects between outputting of the inverted first input signal and the inverted second input signal in response to an externally controllable selection signal and an inverted signal of the selection signal.

The examiner respectfully submits that Freeman clearly discloses in Figure 2 a configuration as cited in the present claim wherein a transmission section (a portion in Figure 2 including 21 and 22 and some other control signals and their inverter) that selects between outputting of the inverted first input signal and the inverted second input signal in response to an externally controllable selection signal and an inverted signal of the selection signal. Let say the output of bar(A) and bar(B) is controlled externally signals (Cs) by either C2 or C3 (C3= bar(C2)) wherein Cs is just a configuration control bits which would be set or preset.

b. The applicant argued in page 10 for claim 8 that Freeman does not disclose the first and second switching sections are provided on the input side of the first and second inversion sections respectively.

The examiner respectfully submits that Freeman clearly discloses the limitations cited in the claim in Figure 2 wherein first and second switching sections are area of configuration including transmission lines of A and B respectively and some other configuration control bits (Cs) for controlling or selecting the switching sections.

c. The applicant argued in page 12 for independent claim 13 that Freeman does not the claimed first and second inversion section including transistor circuits, each transistor circuit having a first and second input signal terminal for the first and second input signal.

The examiner respectfully submits that Freeman discloses in Figure 2 purely a first inversion section including transistor circuits including inverter 21 and one of a dot connection or switching ON/OFF. These basic logic circuits are composed of transistors as its basic structure.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

November 26, 2004

TODD INGBERG
PRIMARY EXAMINER